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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/668,558	09/22/2003	James Stasiak	100201346-5	4709
7590	04/24/2006			EXAMINER WEISS, HOWARD
HEWLETT-PACKARD COMPANY Intellectual Property Administration P. O. Box 272400 Fort Collins, CO 80527-2400			ART UNIT 2814	PAPER NUMBER

DATE MAILED: 04/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

6/1

Office Action Summary	Application No.	Applicant(s)	
	10/668,558	STASIAK ET AL.	
	Examiner	Art Unit	
	Howard Weiss	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 06 February 2006.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-30, 32-34 and 57-59 is/are pending in the application.
 4a) Of the above claim(s) 7-9, 14, 22-30 and 57 is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-6, 10-13, 15-21, 32-34, 58 and 59 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) Notice of References Cited (PTO-892)
 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
 Paper No(s)/Mail Date _____

4) Interview Summary (PTO-413)
 Paper No(s)/Mail Date. _____.
 5) Notice of Informal Patent Application (PTO-152)
 6) Other: _____.

Attorney's Docket Number: 1000201346-5

Filing Date: 9/22/03

Continuing Data: Division of 10/256,984

Claimed Foreign Priority Date: none

Applicant(s): Stasiak et al. (Wu, Hakleman)

Examiner: Howard Weiss

Claim Rejections - 35 USC § 102/103

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Initially, and with respect to Claims 5, 32, 33 and 59, note that a "product by process" claim is directed to the product per se, no matter how actually made. See

In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases as the above case law makes clear.

5. Claims 5, 6, 10 to 13, 15 to 21, 32 to 34, 58 and 59 are rejected under 35 U.S.C. § 102(e) as being anticipated by, or in the alternative, under 35 U.S.C. § 103(a) as obvious over Lieber et al. (U. S. Patent Application Publication No. 2003/0089899 A1).

Lieber et al. show all aspects of the instant invention (e.g. Figures 30 to 39) including:

- a silicon semiconductor wafer and an insulating layer disposed over said wafer (e.g. Figures 34 and 39A)
- a plurality of first doped silicon structures (i.e. base or first semiconductor layer) consisting of parallel conductive lines with a lateral dimension less than about 75 nanometers (Paragraph [00013])
- a plurality of second doped silicon structures (i.e. base or second semiconductor layer) consisting of parallel conductive lines with a lateral dimension less than about 75 nanometers deposited upon said first conductive lines at a 90 degree angle to said first lines

- a first junction formed between said first and second lines of dimensions less than 75 nanometers
- a second set of wires and junctions form on said substrate
- said structures forming diodes or bipolar junction transistors (Paragraph [0200])

As to the grounds of rejection under section 103(a), how the lines are formed, either epitaxial or some other means, pertains to intermediate process steps which do not affect the final device structure. See MPEP § 2113 which discusses the handling of "product by process" claims and recommends the alternative (§ 102 / § 103) grounds of rejection.

6. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lieber et al. and Kitamura (JP 59-106147).

Lieber et al. show most aspects of the instant invention (Paragraph 9) except for the first semiconductor structure having planar top and side surfaces. Kitamura teach (e.g. Figure 1) to have a fist first semiconductor structure **11** having planar top and side surfaces to obtain a high integration density (see Purpose). It would have been obvious to a person of ordinary skill in the art at the time of invention to have a first semiconductor structure having planar top and side surfaces as taught by Kitamura in the device of Lieber et al. to obtain a high integration density.

7. Claims 2 to 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lieber et al. and Kitamura, as applied to Claim 1 above, and further in view of Taussig et al. (U.S. Patent No. 6,552,409).

Lieber et al. and Kitamura show most aspects of the instant invention (Paragraph 10) except for the second structure with the second junction formed on the first structure. Taussig et al. teach (e.g. Figures 23 to 25) to put a second structure **804** on a fist structure **802** to increase the storage capacity (Column 23 Lines 20 to 40). It

would have been obvious to a person of ordinary skill in the art at the time of invention to put a second structure on a first structure as taught by Taussig et al. in the device of Lieber et al. and Kitamura to increase the storage capacity.

Response to Arguments

8. Applicant's arguments filed 2/6/2006 have been fully considered but they are not persuasive. The Applicants dispute that the stated claims have "product-by-product" limitations. As stated in the rejection above, the process limitation is in "epitaxial" which relates to how the semiconductor layers are formed. As defined by Wolf et al. 1986 Page 124, "epitaxial" describes a means of depositing a thin layer of single crystal material on a surface of a single crystal substrate. If the single crystal material and the substrate are the same, it is called homoepitaxy; if they are different, it is called heteroepitaxy. One of ordinary skill in the art would understand that an epitaxial layer is a single crystal layer deposited using an epitaxial method and that the resultant layer has single crystal structure. Therefore, the layers in the prior art that are single crystal in nature would cover this limitation in the claims. As pointed out by the Applicants, the semiconductor layers are deposited by homoepitaxy Si-Si methods and are single crystalline in nature.

In reference to the nanowires not being layers and having a plurality of wires, Lieber et al. states that the wires are in different layers (e.g. Figure 30B), formed as a crossed single-wire array with sets of parallel wires crossed at 90 degrees and formed over a substrate (e.g. Figure 39A). Also, the wires can be doped and form junctions (Paragraph [0200]). In reference to being a "base" or "first" layer, it is the arrangement (i.e. one layer on another) that is anticipated by Lieber et al.

In response to applicant's argument that the planar top and side surfaces could not be incorporated into the device of Lieber et al. because Kitamura use lithography, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the

claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, the Examiner uses Figure 1 of Kitamura showing of the lines having planar top and side surfaces and not how these features are incorporated into the device of Lieber et al. A translation of Kitamura will be forthcoming and made available at a future date.

In view of these reasons and those set forth in the present office action, the rejections of the stated claims stand.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

Art Unit: 2814

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Howard Weiss at **(571) 272-1720** and between the hours of 7:00 AM to 3:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Howard.Weiss@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on **(571) 272-1705**.

12. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at **866-217-9197** (toll-free).

13. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/110, 910	thru 4/17/2006
Other Documentation: none	
Electronic Database(s): EAST, IEL, JPL	thru 4/17/2006

HW/hw
22 July 2005



Howard Weiss
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Art Unit 2814